UNITED STATES PATENT AND TRADEMARK OFFICE

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10/038,431	12/31/2001	Sushma Shrikant Trivedi	04860.P2687	7868

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EXAMINER
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ART UNIT	PAPER NUMBER
2183	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

	Application No.	Applicant(s)
Office Action Summary	10/038,431	TRIVEDI ET AL.
	Examiner	Art Unit	
	Aimee J. Li	2183	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>21 August 2007</u>.

2a)☒ This action is **FINAL**.   2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) <u>1-7, 9-18, 20-32 and 34-41</u> is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) <u>1-7, 9-18, 20-32, and 34-41</u> is/are rejected.

7)☒ Claim(s) <u>25</u> is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on <u>31 December 2001</u> is/are: a)☒ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some *   c)☐ None of:

    1.☐ Certified copies of the priority documents have been received.

    2.☐ Certified copies of the priority documents have been received in Application No. _____.

    3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1.   Claims 1-7, 9-18, 20-32, and 34-41 are pending. Claims 1, 12, 23, 25, and 26 have been

amended as per Applicant's request.

Papers Submitted

2.   It is hereby acknowledged that the following papers have been received and placed of

record in the file: Amendment as filed 21 August 2007.

Claim Objections

3.   Claim 25 is objected to because of the following informalities: Please change claim 25

from "A processing system comprising an execution unit as in claim 23" to --A processing

system comprising an execution unit ~~as in claim 23~~ **comprising...**--, where "..." represents the

rest of the language found in claim 23. This ensures that there will be no confusion as to whether

claim 25 is mean as a dependent or independent claim and what limitations it encompasses.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

4.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in
> section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are
> such that the subject matter as a whole would have been obvious at the time the invention was made to a person
> having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the
> manner in which the invention was made.

5.   Claims 1-3, 5-7, 9-14, 16-18, 20-28, 30-32, 34-38, and 40-41 are rejected under 35

U.S.C. 103(a) as being unpatentable over Chehrazi et al., U.S. Patent No. 6,282,556 (herein

referred to as Chehrazi) in view of Mennemeier et al., U.S. Patent No. 6,036,350 (herein referred

to as Mennemeier).

6.   Regarding claims 1, 12, 23, and 26, taking claim 1 as exemplary, Chehrazi has taught a

method for execution by a microprocessor in response to receiving a single instruction (Chehrazi

Col.20 lines 42-52), the method comprising:

    a.   Receiving a first vector of numbers and a second vector of numbers (Chehrazi

            310 of Fig.20B, Col.20 line 62 – Col.21 line 1);

    b.   Selecting a first plurality of numbers from the numbers in a first vector (Chehrazi

            310 of Fig.20B, Col.20 line 62 – Col.21 line 1) and a second plurality of numbers

            from the numbers in the second vector (Chehrazi 312 of Fig.20B, Col.20 line 62 –

            Col.21 line 1) according to a configuration specified by the instruction (Chehrazi

            560 of Fig 20A, Col.20 line 42 – Col.21 line 13), and

    c.   Generating simultaneously a third plurality of numbers, each of which is an

            absolute difference between a number in the first plurality of numbers and a

            number in the second plurality of numbers (Chehrazi Col.21 lines 6-12),

    d.   Wherein the sum of third plurality of numbers are saved in an entry in a register

            file (Chehrazi Col.20 lines 47-58),

    e.   Wherein the above operations are performed in response to the microprocessor

            receiving the single instruction (Chehrazi Col.20 lines 42-52, 61-62).

7.   Chehrazi has not explicitly taught wherein the third plurality of numbers themselves are

saved in an entry in a register file. However, Mennemeier has taught storing a third plurality of

numbers, specifically a vector of absolute differences, in a instruction specified register

(Mennemeier, Col.7 line 64 – Col.8 line 23) so that the absolute differences can be used in other

operations that require the distance assessment that the results represent (Mennemeier, Col.8 line

21-23). One of ordinary skill in the art would have recognized that it is desirable to retain results

that will be used by future instructions so that the results don't need to be recalculated.

Therefore, one of ordinary skill in the art would have found it obvious to modify the processor of

Chehrazi to store the absolute differences, rather than the sum of the absolute differences, in an

instruction specified register so that the values could be reused by other operations that require

the data, thus improving throughput by avoiding the recalculation of the data.

8.   Claims 12, 23, and 26 are nearly identical to claim 1. However, Chehrazi has taught the

differences. Claim 12 differs in the claim being comprised within a machine-readable media

(Chehrazi Col.20 lines 42-46), while claims 23 and 26 differs in the claims being comprised

within an execution unit (Chehrazi Col.7 lines 20-40). Also, claim 23 claims wherein the

microprocessor is a media processor disposed on an integrated circuit with a memory controller

(Chehrazi column 5, lines 43-54). Besides these differences, the claims encompass the same

scope as claim 1. Thus, claims 12, 23 and 26 are rejected for the same reasons as claim 1.

9.   Regarding claims 2, 13, 24 and 27, taking claim 2 as exemplary, Chehrazi has taught a

method as in claim 1, wherein an absolute difference between a first number and a second

number is computed using a method comprising:

      a.   Producing a first intermediate number by subtracting the second number from the

            first number (Chehrazi Col.21 lines 1-8),

      b.   Producing a second intermediate number by subtracting the first number from the

            second number (Chehrazi Col.21 lines 1-8),

    c.   Selecting a positive number from the first intermediate number and the second

intermediate number as the absolute difference between the first number and the

second number (Chehrazi Col.21 lines 8-12),

    d.   Wherein the microprocessor is a media processor (Chehrazi 108 of Fig.1, Col.3

lines 6-7) disposed on an integrated circuit with a memory controller (Chehrazi

100 of Fig.1, Col.5 lines 46-54).

10.   Claims 13, 24 and 27 are nearly identical to claim 2. Claim 13 lacks the recitation of a

media processor disposed on an integrated circuit with a memory controller, and claims 13, 24

and 27 differ in their parent claims, but encompass the same scope as claim 2. Thus, claims 13,

24 and 27 are rejected for the same reasons as claim 2.

11.   Regarding claims 3, 14 and 28, taking claim 3 as exemplary, Chehrazi has taught a

method as in claim 2, wherein the first intermediate number and the second intermediate number

are produced in parallel (Chehrazi Col.21 lines 1-8), and wherein the third plurality of numbers

are generated substantially simultaneously (Chehrazi Col.21 lines 8-12).

12.   Claims 14 and 28 are nearly identical to claim 3, both differing in their lack of having the

third plurality of numbers being generated substantially simultaneously, as well as differing in

their parent claims, but both encompass the same scope as claim 3. Thus, Claims 14 and 28 are

rejected for the same reasons as claim 3.

13.   Regarding claims 5, 16 and 30, taking claim 5 as exemplary, Chehrazi has taught a

method as in claim 1, wherein the first plurality of numbers are received from a first entry in the

register file (Chehrazi Col.20 lines 47-58).

14.   Claims 16 and 30 are nearly identical to claim 5, differing in their parent claims, but encompassing the same scope as claim 5. Thus, claims 16 and 30 are rejected for the same reasons as claim 5.

15.   Regarding claims 6, 17 and 31, taking claim 6 as exemplary, Chehrazi has taught a method as in claim 5, wherein the single instruction specifies a way to partition a string of bits in the first entry into a first plurality of numbers (Chehrazi Col.20 lines 61-65). Here, the SABD instruction specifies a register in the register file, which corresponds to the plurality of numbers, and specifies that the data in the register be interpreted to be 16 separate 8-bit numbers.

16.   Claims 17 and 31 are nearly identical to claim 6, differing in their parent claims, but encompassing the same scope as claim 6. Thus, claims 17 and 31 are rejected for the same reasons as claim 6.

17.   Regarding claims 7, 18 and 32, taking claim 7 as exemplary, Chehrazi has taught a method as in claim 5, wherein the single instruction specifies an index of the entry in the first register file (Chehrazi 560c and 560d of Fig.20a, Col.20 lines 47-58).

18.   Claims 18 and 32 are nearly identical to claim 7, differing in their parent claims, but encompassing the same scope as claim 7. Thus, claims 18 and 32 are rejected for the same reasons as claim 7.

19.   Regarding claims 9, 20 and 34, taking claim 9 as exemplary, Chehrazi in view of Mennemeier has taught a method as in claim 1, wherein the single instruction specifies an index of the entry in a the register file (Mennemeier, Col.7 line 64 – Col.8 line 23, as well as above paragraph 39).

20.   Claims 20 and 34 are nearly identical to claim 9, differing in their parent claims, but encompassing the same scope as claim 9. Thus, claims 20 and 34 are rejected for the same reasons as claim 9.

21.   Regarding claims 10, 21 and 35, taking claim 10 as exemplary, Chehrazi has taught a method as in claim 1, wherein a type of each of the first and second pluralities of numbers is one of:

    a.   Unsigned integer (Chehrazi Col.20 lines 54-55),

    b.   Signed integer (Chehrazi Col.20 lines 54-55),

    c.   Floating-point number.

22.   Here, because the claim is written in the alternative format, only one of the three possible limitations is required to be met. Thus, Chehrazi has taught the limitations of claim 10.

23.   Claims 21 and 35 are nearly identical to claim 10, differing in their parent claims, but encompassing the same scope as claim 10. Thus, claims 21 and 35 are rejected for the same reasons as claim 10.

24.   Regarding claim 11, 22 and 36, taking claim 11 as exemplary, Chehrazi has taught a method as in claim 1, wherein a size of each of the first and second pluralities of numbers is one of:

    a.   8 bits (Chehrazi Col.20 lines 61-65),

    b.   16 bits,

    c.   32 bits.

25.   Here, because the claim is written in the alternative format, only one of the three possible limitations is required to be met. Thus, Chehrazi has taught the limitations of claim 11.

26.   Claims 22 and 36 are nearly identical to claim 11, differing in their parent claims, but

encompassing the same scope as claim 11. Thus, claims 22 and 36 are rejected for the same

reasons as claim 11.

27.   Regarding claim 25, Chehrazi has taught a processing system comprising an execution

unit as in claim 23 (Chehrazi Fig.1).

28.   Regardin claim 37, Chehrazi has taught wherein a type of each of the first and second

pluralities of numbers is floating point number (Chehrazi column 1, lines 19-21 and column 9,

lines 37-41).

29.   Regarding claim 38, Chehrazi has taught wherein the microprocessor is a media

processor disposed on an integrated circuit with a memory controller (Chehrazi column 5, lines

43-54).

30.   Regarding claim 40, Chehrazi has taught wherein the memory controller is usable to

access memory not disposed on the integrated circuit (Chehrazi Col. 5 lines 36-60 and Figure 1).

As can be seen in Chehrazi's Figure 1, the ROM and RAM memories and data storage device are

separate from the processor.

31.   Regarding claim 41, Chehrazi has taught wherein the memory controller is usable by a

host central processing unit not disposed on the integrated circuit to access the memory

(Chehrazi Col. 5 lines 36-60 and Figure 1). As can be seen in Chehrazi's Figure 1, the ROM and

RAM memories and data storage device are separate from the processor.

32.   Claims 4, 15, 29, and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Chehrazi et al., U.S. Patent No. 6,282,556 (herein referred to as Chehrazi) in view of

Mennemeier et al., U.S. Patent No. 6,036,350 (herein referred to as Mennemeier) as applied to

claims 1, 2, 12, 26, and 27 above, and further in view of Diefendorff et al., EPO 0 485 776 A2 (herein referred to as Diefendorff).

33.   Regarding claims 4, 15, 29, and 39, taking claim 4 as exemplary, Chehrazi has taught taking an absolute difference between a first number and a second number (Chehrazi Col.21 lines 6-12). Chehrazi has not taught:

      a.   Testing if an overflow occurs in producing the first intermediate number and the second intermediate number,

      b.   Saturating the difference between the first number and the second number if an overflow occurs.

34.   Diefendorff has taught

      a.   Testing if an overflow occurs in producing the first intermediate number and the second intermediate number (Diefendorff column 6, lines 42-46; column 11, lines 38-41; column 11, line 56 to column 12, line 12; and Figure 5),

      b.   Saturating the difference between the first number and the second number if an overflow occurs (Diefendorff column 6, lines 42-46; column 11, lines 38-41; column 11, line 56 to column 12, line 12; and Figure 5).

35.   A person of ordinary skill in the art at the time the invention was made would have recognized, and as taught by Diefendorff, that overflow testing and saturation arithmetic improves the handling of overflow conditions during shading or image processing, thereby improving the quality of the image and accelerating the performance of the microprocessor during shading and image processing. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the overflow testing

and saturation arithmetic of Diefendorff in the device of Chehrazi to improve image quality and

accelerate the performance of a microprocessor during shading and image processing.

Response to Arguments

36.   Applicant's arguments filed 21 August 2007 have been fully considered but they are not

persuasive.

37.   Applicant's argue in essence on page 13-14

> ...It is respectfully submitted that Chehrazi does not teach or suggest a
>
> combination with Mennemeier, and Mennemeier does not teach or suggest a
>
> combination with Chehrazi. It would be impermissible hindsight, based on
>
> applicants' own disclosure, to combine Chehrazi and Mennemeier...

38.   This has not been found persuasive. As recited previous rejection copied above,

Mennemeier has taught in column 8, lines 21-23 that storing absolute differences in a specified

register, i.e. register in a register file, allows the absolute differences to be used in other

operations that require the distance assessment that the results represent. As such, there is a

teaching or suggestion to combine Mennemeier into Chehrazi, since Chehrazi has not taught

storing the absolute differences in a specified register. In response to applicant's argument that

the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be

recognized that any judgment on obviousness is in a sense necessarily a reconstruction based

upon hindsight reasoning. But so long as it takes into account only knowledge which was within

the level of ordinary skill at the time the claimed invention was made, and does not include

knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In*

re McLaughlin, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

39.   Applicant's argue in essence on pages 13-16

> ...It is respectfully submitted that neither Chehrazi, Mennemeier, nor Diefendorff
>
> disclose generating <u>simultaneously</u> a third plurality of numbers, <u>each of which is</u>
>
> <u>an absolute difference between a number in the first plurality of numbers and a</u>
>
> <u>number in the second plurality of numbers</u>, as recited in amended claim 1...

40.   This has not been found persuasive. The passage Applicants' relied upon to support their

arguments states "This simultaneously products 32 separate differences and a positive and a

negative difference for each corresponding operand pair. Multiplexers in circuit 332 then select

the positive difference for each operand pair as the absolute value difference for each pair."

Applicants' arguments are assuming that, since this passage only uses the word "simultaneously"

in the sentence stating the 32 separate differences are calculated simultaneously, the absolute

difference selected by the multiplexers does not occur simultaneously. However, this does not

make sense for Chehrazi's system. If the intermediate positive and negative differences are

found simultaneously, all results are fed into the multiplexers in circuit 332 simultaneously, since

the results are found simultaneously. It stands to reason that the plurality of multiplexers in

circuit 332 selecting the final absolute difference for each operand pair operate simultaneously.

If the plurality of multiplexers in circuit 332 were to select the absolute differences individually,

as suggested by Applicants' arguments, then there would be no necessity for the system to have a

plurality of multiplexers. Only a single multiplexer would be needed.

41.   Also, the claim language uses the word "comprising", making it open not closed. So, the

prior art simply needs to teach that the absolute differences are part of the third plurality of

numbers generated. Chehrazi has taught that both the positive and negative differences are

simultaneously found between the two operands, and the positive difference is the final absolute difference result.

Conclusion

42.   The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

    a.   Aono et al.'s "A Video Digital Signal Processor with a Vector-Pipeline Architecture" from <u>IEEE Journal of Solid-State Circuits, Volume 27, Number 12 December 1992</u> ©1992 has taught a special ALU that not only performs basic arithmetic and logic operations but calculates absolute differences for vectors.

    b.   Kohn et al.'s "The Visual Instruction Set (VIS) in UltraSPARC™" ©1995 IEEE has taught a single PDIST instruction for finding the absolute difference of two vectors.

43.   **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

44.   A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

45.   Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Aimee J. Li whose telephone number is (571) 272-4169. The

examiner can normally be reached on M-T 7:00am-4:30pm.

46.   If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the

organization where this application or proceeding is assigned is 571-273-8300.

47.   Information regarding the status of an application may be obtained from the Patent

Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR

system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would

like assistance from a USPTO Customer Service Representative or access to the automated

information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Aimee J Li
Examiner
Art Unit 2183

29 October 2007